Docket No.: 057810-0025

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Ryosuke USUI, et al.	:	Confirmation Number: 4232
Application No.: 09/985,743	:	Tech Center Art Unit: 2815
Filed: November 06, 2001	:	Examiner: Lee, Eugene

For: SEMICONDUCTOR DEVICE HAVING ELEMENT ISOLATION TRENCH AND METHOD OF FABRICATING THE SAME

TRANSMITTAL OF SUBSTITUTE APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Non-Compliant Appeal Brief dated October 25, 2006, submitted herewith is Appellant's Substitute Appeal Brief in support of the Notice of Appeal filed July 11, 2006. The Appeal Brief fee of $500.00 has already been charged to Deposit Account 500417. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Brian K. Seidleck
Registration No. 51,321

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BKS:idw
Facsimile: 202.756.8087
Date: **November 7, 2006**

TABLE OF CONTENTS

Docket No.: 057810-0025 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Ryosuke USUI, et al.	:	Confirmation Number: 4232
Application No.: 09/985,743	:	Tech Center Art Unit: 2815
Filed: November 06, 2001	:	Examiner: Lee, Eugene

For: SEMICONDUCTOR DEVICE HAVING ELEMENT ISOLATION TRENCH AND METHOD OF FABRICATING THE SAME

SUBSTITUTE APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Substitute Appeal Brief is submitted in support of the Notice of Appeal filed July 11, 2006 and in response to the Notification of Non-Compliant Appeal Brief mailed October 25, 2006, wherein Appellant appeals from the Primary Examiner's rejection of claims 1, 2, 6 and 18.

I. Real Party In Interest

This application is assigned to Sanyo Electric Co., Ltd., by assignment recorded on November 6, 2001, at Reel 012298, Frame 0191.

II. Related Appeals and Interferences

Appellant is unaware of any related Appeal or Interference.

III. Status of Claims

Claims 1, 2, 6 and 18, which are reproduced in the Claim Appendix, stand twice rejected and are subject to this Appeal. Claims 3, 4, 5 and 7 were previously cancelled and claims 8-17 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b).

IV. Status of Amendments

No amendment has been filed since the Office action dated February 13, 2006. Hence, there is no outstanding amendment that has not been entered.

V. Summary of Claimed Subject Matter

The present claimed subject matter relates to a semiconductor device having an element isolation trench (page 1, lines 6-10 of the specification). An object of the present claimed subject matter is to provide a semiconductor device capable of preventing defective embedding of an insulator in the element isolation trench and improving the withstand voltage (dielectric strength) of an element isolation region (page 3, lines 1-5 of the specification).

Independent claim 1 describes a semiconductor device comprising an element isolation trench 111 that is formed on the main surface of the semiconductor substrate 10. The element isolation trench 111 is substantially filled with an insulator 112. As shown in FIG. 9, the trench width of an upper end of the element isolation trench 111 is larger than the trench width of a bottom surface, while the length of a side surface located between the upper end and an end of the bottom surface is larger than the length of a straight line connecting the upper end and the end of the bottom surface. The side surface of the element isolation trench includes a first side surface 111a located in the vicinity of the upper end of the element isolation trench 111 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate, as shown in FIG. 9. A second side

surface 111c is located in the vicinity of the bottom surface of the element isolation trench 111 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate. A substantially single, straight and linearly inclined third side surface 111b directly connects the first side surface 111a and the second side surface 111c with each other (page 21, lines 11-21 of the specification).

Independent claim 2 describes a semiconductor device comprising an element isolation trench 111 that is formed on the main surface of the semiconductor substrate 10. The element isolation trench 111 is substantially filled with an insulator 112. As shown in FIG. 9, the trench width of an upper end of the element isolation trench 111 is larger than the trench width of a bottom surface, while the length of a side surface located between the upper end and an end of the bottom surface is larger than the length of a straight line connecting the upper end and the end of the bottom surface. The side surface of the element isolation trench includes a first side surface 111a located in the vicinity of the upper end of the element isolation trench 111 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate, as shown in FIG. 9. A second side surface 111c is located in the vicinity of the bottom surface of the element isolation trench 111 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate. A substantially inclined third side surface 111b directly connects the first side surface 111a and the second side surface 111c with each other. Independent claim 2 requires that the section of at least a central portion of the side surface of the element isolation trench 111 exhibits a substantially curvilinear S shape (FIG. 1) having an angle of inclination gradually steepened toward a downward direction perpendicular to the main surface of the semiconductor substrate 10 (page 15, lines 10-21 of the specification).

Independent claim 18 describes a semiconductor device comprising an element isolation trench 11 formed on the main surface of a semiconductor substrate 10, as shown in FIG. 1. The element isolation trench 11 is substantially filled with an insulator 12. The trench width of an upper end of the element isolation trench 11 is larger than the trench width of a bottom surface. The trench comprises a first side surface 11a located in the vicinity of the upper end of the element isolation trench 11 and is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate 10. A second side surface 11c is located in the vicinity of the bottom surface of the element isolation trench 11 and is formed to be substantially perpendicular to the main surface of the semiconductor substrate 10. A third side surface 11b directly connects the first side surface 11a and the second side surface 11c with each other. The third side surface 11b is substantially single, straight and linearly inclined (FIG. 9) with respect to the main surface **or** exhibits a substantially curvilinear S shape (FIG. 1) having an angle of inclination gradually steepened toward a downward direction perpendicular to the main surface of the semiconductor substrate 10. See page 15, lines 10-21 and page 21, lines 11-21 of the specification.

VI. Grounds of Rejection To Be Reviewed On Appeal

The Rejection:

Claims 1, 2, 6 and 18 were rejected under 35 U.S.C. § 102(b) as being unpatentable over Jang (U.S. Pat. No. 5,910,018, hereinafter "Jang").

The issue which arises in this Appeal and requires resolution by the Honorable Board of Patent Appeals and Interferences is whether claims 1, 2, 6 and 18 are unpatentable under 35 U.S.C. § 102 for anticipation predicated upon Jang.

VII. Argument

Examiner's Position

The Examiner, at page 2 of the February 13, 2006 Office action stated that Jang, at Figure 9, teaches all of the limitations of claims 1, 2, 6 and 18. The Examiner included a marked-up version of Fig. 9 of Jang at page 2 of the final Office action, wherein three circled areas allegedly correspond to the first, second and third surfaces of the instant claims.

In the Advisory Action dated June 8, 2006, the Examiner asserted that the first side surface of Jang includes the perpendicular surface and a curved surface, as shown in FIG. 9. The Examiner asserted that the claim does not state that the entire first side surface must be perpendicular, but rather only formed substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate.

Appellant's Position

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention under any statutory provision always rests upon the Examiner. *In re Mayne*, 41 USPQ2d 1451 (Fed. Cir. 1997); *In re Duel*, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Bell*, 26 USPQ2d 1529 (Fed. Cir. 1993). Appellant submits that this burden has not been established.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Moreover, in imposing the rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an

applied reference is perceived to identically disclose each feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). There are significant differences between the claimed subject matter and the device disclosed by Jang that scotch the factual determination that Jang identically describes the claimed inventions within the meaning of 35 U.S.C. § 102.

Each of independent claims 1, 2 and 18 recites a semiconductor device including a first surface located in the vicinity of the upper end of the element isolation trench. The first surface is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate. In contrast, Jang at col. 3, line 61 through col. 4, line 7 discloses a silicon substrate 10 having a trench 50, as shown in Fig. 9. The trench 50 has a lower portion 52 with vertical side walls 54. The trench 50 also has an upper portion 60 having rounded edges 62 formed by oxide 28. Jang's two piece/portion trench is clearly illustrated in FIG. 5 which depicts the upper portion (round surfaces) formed, followed by the lower portion (vertical sides) formed in FIG. 6.

Contrary to the express teachings of the Jang reference, the Examiner asserted that Jang discloses a first side surface that is perpendicular. See page 2 of the February 13, 2006 final Office action. The region identified by the Examiner that allegedly corresponds to the first surface of the present application, is actually part of Jang's an upper portion 60 which includes rounded edges 62. Thus, contrary to the Examiner's assertion, Jang fails to disclose or remotely suggest a first surface that is formed to be substantially perpendicular to and extending downwardly from the main surface of the semiconductor substrate. Accordingly, the rejection under 35 U.S.C. § 102 is not legally viable for at least this reason.

Further, since Jang explicitly teaches that the trench 50 has a lower portion 52 with vertical side walls 54 and an upper portion 60 with rounded edges 62, the reference fails to disclose a third surface, much less a third surface that directly connects a first and second side surface, as required in each of independent claims 1, 2 and 18. Indeed, as Jang expressly states at col. 3, line 61 through col. 4, line 7, trench 50 is composed of two surfaces – vertical side walls 54 directly connected to rounded side walls 62. Thus, each of independent claims 1, 2 and 18 are free from the applied art for at least this reason.

Moreover, each of independent claims 1, 2 and 18 requires an element isolation trench substantially filled with an insulator. Jang, on the other hand, discloses that trench 50 is substantially filled with a dielectric material 30 (FIG. 7). See Jang at col. 4, lines 6-7.

Furthermore, independent claim 2 requires that the section of at least a central portion of the side surface of the element isolation trench exhibits a substantially curvilinear S shape having an angle of inclination gradually steepened toward a downward direction perpendicular to the main surface of the semiconductor substrate. It is not apparent where the portion identified by the Examiner is a substantially curvilinear S shape as claimed. Jang explicitly teaches that the trench 50 has a lower portion 52 with vertical side walls 54 and an upper portion 60 with rounded edges 62. The combination of the vertical side walls 54 with the rounded edges 62 does not form a substantially curvilinear S shape.

Based upon the arguments submitted supra, Appellant submits that the Examiner's rejection under 35 U.S.C. § 102 is factually and legally erroneous. The above argued differences between the claimed semiconductor device and that of the Jang reference undermines the factual determination that Jang discloses the device identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 U.S.P.Q. 86 (Fed. Cir. 1986).

Appellant, therefore, solicits the Honorable Board to reverse the Examiner's rejection under 35 U.S.C. § 102.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Brian K. Seidleck
Registration No. 51,321

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BKS:idw
Facsimile: 202.756.8087

Please recognize our Customer No. 20277 as our correspondence address.

Date: November 7, 2006

VIII. CLAIM APPENDIX

1. A semiconductor device comprising:

a semiconductor substrate having a main surface; and

an element isolation trench formed on said main surface of said semiconductor substrate, said element isolation trench being substantially filled with an insulator, wherein

the trench width of an upper end of said element isolation trench is larger than the trench width of a bottom surface while the length of a side surface located between said upper end and an end of said bottom surface is larger than the length of a straight line connecting said upper end and said end of said bottom surface, and

said side surface of said element isolation trench includes:

a first side surface located in the vicinity of said upper end of said element isolation trench and formed to be substantially perpendicular to and extending downwardly from said main surface of said semiconductor substrate,

a second side surface located in the vicinity of said bottom surface of said element isolation trench and formed to be substantially perpendicular to said main surface of said semiconductor substrate, and

a substantially single, straight and linearly inclined third side surface directly connecting said first side surface and said second side surface with each other.

2. A semiconductor device comprising:

a semiconductor substrate having a main surface; and

an element isolation trench formed on said main surface of said semiconductor substrate, said element isolation trench being substantially filled with an insulator, wherein

the trench width of an upper end of said element isolation trench is larger than the trench width of a bottom surface while the length of a side surface located between said upper end and an end of said bottom surface is larger than the length of a straight line connecting said upper end and said end of said bottom surface, and

said side surface of said element isolation trench includes:

a first side surface located in the vicinity of said upper end of said element isolation trench and formed to be substantially perpendicular to and extending downwardly from said main surface of said semiconductor substrate,

a second side surface located in the vicinity of said bottom surface of said element isolation trench and formed to be substantially perpendicular to said main surface of said semiconductor substrate, and

a substantially inclined third side surface directly connecting said first side surface and said second side surface with each other, wherein

the section of at least a central portion of said side surface of said element isolation trench exhibits a substantially curvilinear S shape having an angle of inclination gradually steepened toward a downward direction perpendicular to said main surface of said semiconductor substrate.

6. The semiconductor device according to claim 1, wherein

the third side surface is linearly inclined with respect to the main surface of the semiconductor substrate.

18. A semiconductor device comprising:

a semiconductor substrate having a main surface; and

an element isolation trench formed on said main surface of said semiconductor substrate, said element isolation trench being substantially filled with an insulator, wherein

the trench width of an upper end of said element isolation trench is larger than the trench width of a bottom surface, the trench comprising:

a first side surface located in the vicinity of said upper end of said element isolation trench and formed to be substantially perpendicular to and extending downwardly from said main surface of said semiconductor substrate,

a second side surface located in the vicinity of said bottom surface of said element isolation trench and formed to be substantially perpendicular to said main surface of said semiconductor substrate, and

a third side surface, directly connecting said first side surface and said second side surface with each other, which is substantially single, straight and linearly inclined with respect to the main surface or exhibits a substantially curvilinear S shape having an angle of inclination gradually steepened toward a downward direction perpendicular to said main surface of said semiconductor substrate.

IX. EVIDENCE APPENDIX

Not applicable.

X. RELATED PROCEEDINGS APPENDIX

Not applicable. Appellant is unaware of any related proceedings.